CLAIMS

1. A transistor for active matrix display comprising a microcrystalline silicon film (5) and an insulator (3), the crystalline fraction being above 80%,

wherein it comprises a plasma treated interface (4) located between the insulator (3) and the microcrystalline silicon film (5) so that the said transistor (1) has a linear mobility equal or superior to 1.5 $cm^2V^{-1}s^{-1}$, shows threshold voltage stability and wherein the microcrystalline silicon film (5) comprises grains (6) whose size ranges between 10 nm and 400 nm.

2. A transistor for active matrix display according to claim 1, wherein said grain size ranges between 100 nm and 200 nm.

3. A transistor for active matrix display according to claim 1 or 2, wherein the microcrystalline silicon film (5) thickness is comprised between 100 nm and 450 nm.

4. A transistor for active matrix display according to any one of claims 1 to 3, wherein said transistor (1) has a top-gate electrode.

5. A transistor for active matrix display according to any one of claims 1 to 3 wherein said transistor (1) has a bottom-gate electrode.

6. A display unit having a line-column matrix of pixels that are actively addressed, wherein each pixel comprises at least a transistor (1) according to any one of claims 1 to 5.

7. A display unit according to claim 6, wherein said pixels comprise light emissive organic materials.

8. A display unit according to claim 6, wherein said pixels comprise liquid crystals.

9. A display unit according to claim 6, wherein said pixels comprise light emissive polymer materials.

10. A display unit according to any one of claims 6 to 9, wherein electronic control means to drive each pixel are at least partially integrated on the corresponding microcrystalline silicon film.

11. A method for producing a transistor for active matrix display comprising the steps of forming an active material and electrodes (2), said active material being formed using vapor deposition methods and said transistor (1) comprising an insulator (3),

wherein,

- forming a plasma treated interface (4) on top of said insulator (3), and

- forming a microcrystalline film (5) on top of said treated interface (4) at a temperature comprised between 100 and 400°C using at least a deposition chemical element and a crystallisation chemical element wherein the said crystalline fraction being above 80% and said microcrystalline silicon film (5) comprises grains (6) where size ranges between 10 nm and 400 nm.

12. A method for producing a transistor according to claim 11, wherein said plasma treated interface (4) is selected from the group consisting of a SiN_x layer, a SiN_xO_y layer, a SiO_2 layer and glass.

13. A method for producing a transistor according to claim 12, wherein one forms the plasma treated interface (4) using a gas selected from the group consisting of N_2, O_2, N_2O and NH_3.

14. A method for producing a transistor according to one of claims 11 to 13, wherein the microcrystalline silicon film (5) is formed using a buffer gas selected from the group consisting of Ar, Xe, Kr and He.

15. A method for producing a transistor according to any of the claims 11 to 14, wherein said crystallisation chemical elements is H_2.

16. A method for producing a transistor according to one of claims 11 to 15, wherein said deposition chemical elements are selected among the group comprising SiH_4, SiF_4.

17. A method for producing a transistor according to one of claims 11 to 16, wherein said deposition chemical elements flux and said crystallisation chemical elements flux are at equilibrium during the growth of the microcrystalline silicon film.

18. A method for producing a transistor according to any one of claims 11 to 17, wherein one forms a top gate transistor.

19. A method for producing a transistor according to claim 18, wherein one patterns the substrate comprising a metallic layer to form source and drain electrodes.

20. A method for producing a transistor according to any one of claims 11 to 17, wherein one forms a bottom gate transistor.

21. A method for producing a transistor according to claim 20, wherein the substrate comprises a gate electrode.

22. A method for producing a transistor according to any one of claims 11 to 21, wherein the microcrystalline silicon film (5) comprises grains (6) whose size ranges between 10 nm and 400 nm.

23. A method for producing a transistor according to any one of claims 11 to 22, wherein the microcrystalline silicon film (5) thickness is comprised between 100 nm and 450 nm.

24. A method for producing a transistor according to any one of claims 11 to 23, wherein the microcrystalline silicon film (5) is produced by hot wire technique.

25. A method for producing a transistor according to any one of claims 11 to 24, wherein the microscrystalline silicon film (5) is produced by radiofrequency glow discharge technique.

26. A method for producing a transistor according to any one of claims 11 to 25, wherein the vapor deposition methods use radiofrequency glow discharge technique.

27. A method for producing a transistor according to claim 26, wherein one uses a 13.56 MHz PECVD reactor.